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block 800 immediately deactivates the selection signal Rough_lock_flag that controls the shift multiplexer to thereby make the careful delay controller 410 not be used.

Paragraph beginning at page 15, line 10:

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As described above, in a delay locked loop of a semiconductor memory device in accordance with the present invention, by using different circuits depending on whether the locking is completed or not, i.e., using the careful delay controller when the locking is accomplished and not using the careful delay controller when the locking is not completed, it is possible to obtain a short locking time when the locking is not accomplished and to reduce an incorrect locking determination due to noise by using the careful delay controller when the locking is done.

IN THE CLAIMS:

Please amend claims 1-6 as follows:

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1. (Amended) A delay locked loop for use in a semiconductor memory device, comprising:

a controllable delay chain means for controlling a delay time of a clock signal coupled thereto;

a comparison means for comparing a reference clock signal with a delayed clock signal generated from the controllable delay chain means and detecting a need for an increase or decrease of the delay time; and

an instant locking delay control means for detecting whether a locking between the reference clock signal and the delayed clock signal is accomplished,

wherein, when the locking is accomplished, the instant locking delay control means is operated to compensate for noise detected by the comparison means and to control the controllable delay chain means, and

wherein, when the locking is not accomplished, the instant locking delay control means is not operated to compensate for noise and the output signals generated by the comparison means are used to directly control the controllable delay chain means.

2. (Amended) The delay locked loop of claim 1, wherein the instant locking delay control means includes:

a delay controller for counting a number of times the output signal of the comparison means is activated and generating a signal requesting an increase or decrease of the delay time if the counted number is larger than a predetermined value;

a locking detector for detecting, in response to the reference clock signal and the delayed clock signal, whether the locking is accomplished and generating a selection signal representing whether the locking is accomplished; and

a shift multiplexer for selectively outputting one of the output signal of the comparison means and the output signal of the delay controller in response to the selection signal, thereby controlling the controllable delay chain means.

3. The delay locked loop of claim 2, wherein the locking detector comprises:

a first delay unit for delaying the delayed clock signal by a predetermined time to thereby generate a delayed output signal;

a second delay unit for delaying the reference clock signal by a preset time to thereby produce a delayed reference clock signal;

a first determination unit for determining, in response to the reference clock signal and the delayed output signal, whether the delayed output signal is slower than the reference clock signal;

a second determination unit for deciding, in response to the delayed clock signal and the delayed reference clock signal, whether the delayed reference clock signal is slower than the delayed clock signal; and

a logic unit for generating the selection signal based on output signals of the first and the second determination units.

4. The delay locked loop of claim 3, wherein the locking detector further comprises an output unit for delaying, in response to the reference clock signal, an

output signal of the logic unit when the locking is accomplished, to thereby control the shift multiplexer.

5. The delay locked loop of claim 4, wherein the output unit comprises:

a plurality of shift registers configured to shift the output signal of the logic unit and to be reset;

a NAND gate for performing a negative AND operation for shifted values of the plurality of shift registers;

and an inverter for producing the selection signal by inverting an output of the NAND gate.

6. The delay locked loop of claim 4, wherein the output unit comprises:

a plurality of shift registers configured to receive the output signal of the logic unit as their reset signal and to shift a high data value input to a first of the registers; and

an output means for generating a data value output from the last one of the shift registers as the selection signal.

Please add claims 7-18 as follows:

7. (New) In a delay locked loop, a delay control circuit for generating a control signal for causing an increase or decrease in a delay time of a delayed clock signal, comprising:

a time-offset detector coupled to the delayed clock signal and a reference clock signal and configured to generate a first adjustment signal indicating a need for an increase or decrease of the delay time;

a delay controller coupled to the first adjustment signal and configured to generate a second adjustment signal by applying noise compensation to the first adjustment signal;

a locking detector coupled to the delayed clock signal and the reference signal and configured to assert a lock signal when a locking condition is satisfied; and

a selector configured to provide one of the first and second adjustment signals as the control signal in response to the lock signal.

8. (New) The delay control circuit of claim 7, wherein the selector comprises a shift multiplexer having first and second input terminals coupled to receive the first and second adjustment signals respectively, and a control terminal coupled to receive the lock signal.

9. (New) The delay control circuit of claim 7, wherein the locking detector comprises:

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a first delay unit configured to further delay the delayed clock signal;

a second delay unit configured to delay the reference clock signal;

a first time-offset detector coupled to receive the reference clock signal and an output signal of the first delay unit and configured to assert a first flag signal when the output of the first delay unit arrives after the reference clock signal;

a second time-offset detector coupled to receive the delayed clock signal and an output signal of the second delay unit and configured to assert a second flag signal when the output of the second delay unit arrives after the delayed clock signal; and

a delay logic block coupled to receive the first and second flag signals and to assert a third flag signal when both the first and second flag signals are asserted, the third flag signal indicating whether the locking condition is achieved.

10. (New) The delay control circuit of claim 9, wherein the first time-offset detector comprises:

a first latch configured to detect falling edges of the reference clock signal and the output signal of the first delay unit;

a second latch having input terminals coupled to respective output terminals of the first latch and an enable terminal;

a pulse generator, responsive to the reference clock signal, having an output terminal coupled to the enable terminal of the second latch; and

a third latch having input terminals coupled to respective output terminals of the second latch and an output terminal that provides the first flag signal.

11. (New) The delay control circuit of claim 9, wherein the delay logic block comprises:

a first inverter configured to invert the first flag signal;

a NAND gate having a first input terminal coupled to receive the inverted first flag signal, a second input terminal coupled to receive the second flag signal, and an output terminal; and

a second inverter having an input terminal coupled to the output terminal of the NAND gate and an output terminal that provides the third flag signal.

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12. (New) The delay control circuit of claim 9, wherein the locking detector further comprises an output generator coupled to receive the third flag signal and to delay transmission of a locked state of the third flag signal while not delaying transmission of an unlocked state of the third flag signal.

13. (New) The delay control circuit of claim 12, wherein the output block comprises:

a plurality of serially coupled shift registers, each having a control terminal coupled to receive the reference clock signal, a reset terminal, a data input terminal, and an output terminal, the data input terminal of a first shift register in the plurality of shift registers being coupled to receive the third flag signal; and

a NAND gate having a respective input terminal coupled to the output terminal of each of the plurality of shift registers, the NAND gate causing the locked state of the third flag signal to be transmitted only when the locked state is shifted through all of the plurality of shift registers.

14. (New) The delay control circuit of claim 12, wherein the output block comprises:

a plurality of serially coupled shift registers, each having a control terminal coupled to receive the reference clock signal, a reset terminal coupled to receive the third flag signal, a data input terminal, and a data output terminal, the data input terminal of a first shift register in the plurality of shift registers having its data terminal coupled to receive a logic high signal,

wherein the unlocked state of the third flag signal causes each of the plurality of shift registers to be reset.

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15. (New) In a delay locked loop circuit having a delay chain, a method of providing a delay adjustment signal for controlling a delay time, comprising:

comparing a delayed clock signal generated by the delayed chain to a reference signal, thereby generating a first adjustment signal;

applying a noise-compensating condition to the first adjustment signal, thereby generating a second adjustment signal;

comparing the delayed clock signal and the reference signal, thereby generating a locking signal;

when the locking signal is in a locked state, selecting the second adjustment signal as the delay adjustment signal; and

when the locking signal is in an unlocked state selecting the first adjustment signal as the delay adjustment signal.

16. (New) The method of claim 15, wherein applying a noise-compensating condition to the first adjustment signal comprises:

counting a number of occurrences of the first adjustment signal; and

generating the second adjustment signal when the number of occurrences exceeds a predetermined threshold.

17. (New) The method of claim 15, wherein comparing the delayed clock signal and the reference signal comprises:

delaying the reference signal by a predetermined time;

comparing the delayed clock signal to the delayed reference signal;

generating a first flag signal when the delayed clock signal arrives later than the reference clock signal;

delaying the delayed clock signal by a predetermined time, thereby producing a second delayed clock signal;

comparing the reference signal to the second delayed clock signal;

generating a second flag signal when the reference signal arrives later than the delayed clock signal; and

generating the locking signal based on the first and second flag signals.

18. (New) The method of claim 15, further comprising:

delaying for a predetermined time a transition of the locking signal to a locked state, while not delaying a transition of the locking signal to an unlocked state.

IN THE DRAWINGS:

Submitted herewith is one amended drawing sheet on which proposed amendments to Fig. 4 have been indicated in red ink. It is respectfully submitted that no new matter has been added.